AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of fabricating a thin film transistor comprising the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity on the surface of said amorphous silicon layer;

forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer;

subsequently, removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance, and wherein in a sectional view said channel region in said amorphous silicon layer is convex with respect to said contact layer; and

removing the impurity formed over the amorphous silicon layer in the channel region between the drain and source electrodes while retaining the impurity over the amorphous silicon [[film]] layer surface contacted with drain and source region, so that the drain and source regions become a contact layer.

2. (Original) The method of claim 1 wherein said contact layer contains a concentration of said impurity of at least 0.01 %.

3. (Currently amended) [[A]] The method of ~~fabricating a thin film transistor comprising the steps of:~~ claim 1,

~~providing a gate over a substrate;~~

~~providing a gate insulating layer over said gate and said substrate;~~

~~providing an amorphous silicon layer having a first resistance over said gate insulating layer;~~

~~providing an impurity on the surface of said amorphous silicon layer;~~

~~forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer;~~

~~subsequently, removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance, and~~

wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma~~; and~~

~~removing the impurity formed over the amorphous silicon in the channel region between the drain and source electrodes while retaining the impurity over the amorphous silicon film surface contacted with drain and source region, so that the drain and source regions become a contact layer~~.

4. (Cancelled).

5. (Currently amended) [[A]] The method of ~~fabricating a thin film transistor comprising the steps of:~~ claim 1.

~~providing a gate over a substrate;~~

~~providing a gate insulating layer over said gate and said substrate;~~

~~providing an amorphous silicon layer having a first resistance over said gate insulating layer;~~

~~providing an impurity on the surface of said amorphous silicon layer;~~

~~forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; and~~

~~subsequently, removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance, and~~

wherein said diffusion of said impurity into said contact portion is performed by heat annealing~~; and~~

~~removing the impurity formed over the amorphous silicon in the channel region between the drain and source electrodes while retaining the impurity over the amorphous silicon film surface contacted with drain and source region, so that the drain and source regions~~ become ~~a contact layer~~.

6. (Cancelled).

7. (Original) The method of claim 1 wherein said impurity is phosphorus.

8. (Currently Amended) The method of claim 1 wherein said amorphous silicon [[film]] layer is deposited to a thickness of about 150 nm - 200 nm.

9. – 12. (Cancelled).

13. (Currently Amended) A method of fabricating a thin film transistor comprising the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity over said amorphous silicon layer, wherein said amorphous silicon layer does not contain said impurity;

etching said silicon layer utilizing a common photoresist to form a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer;

subsequently, removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance, and wherein in a sectional view said channel region in said amorphous silicon layer is convex with respect to said contact layer; and

removing the impurity formed over the amorphous silicon layer in the channel region between the drain and source electrodes while retaining the impurity over the amorphous silicon [[film]] layer surface contacted with drain and source region, so that the drain and source regions become a contact layer.

14. (Original) The method of claim 13 wherein said contact layer contains a concentration of said impurity of at least 0.01 %.

15. (Original) The method of claim 13 wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

16. (Cancelled).

17. (Original) The method of claim 13 wherein said diffusion of said impurity into said contact region is performed by heat annealing.

18. (Cancelled).

19. (Original) The method of claim 13 wherein said impurity is phosphorus.

20. (Currently Amended) The method of claim 13 wherein said amorphous silicon [[film]] layer is deposited to a thickness of about 150 nm - 200 nm.

21. – 23. (Cancelled).

24. (Currently Amended) A method of fabricating a thin film transistor comprising the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity on the surface of said amorphous silicon layer;

providing a photoresist over said impurity and back exposing said photoresist utilizing said gate stack as a mask and developing a pattern substantially identical with that of said gate;

removing said pattern and forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer;

subsequently, removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance, and wherein essentially none of said impurity is diffused into said contact portion prior to said removing step, and wherein in a sectional view said

channel region in said amorphous silicon layer is convex with respect to said contact layer; and

removing the impurity formed over the amorphous silicon layer in the channel region between the drain and source electrodes while retaining the impurity over the amorphous silicon [[film]] layer surface contacted with drain and source region, so that the drain and source regions become a contact layer.

25. (Original) The method of claim 24 wherein said contact layer contains a concentration of said impurity of at least 0.01%.

26. (Original) The method of claim 24 wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

27. (Cancelled).

28. (Original) The method of claim 24 wherein said diffusion of said impurity into said contact region is performed by heat annealing.

29. (Cancelled).

30. (Original) The method of claim 24 wherein said impurity is phosphorus.

31. (Currently Amended) The method of claim 24 wherein said amorphous silicon [[film]] layer is deposited to a thickness of about 150 nm - 200 nm.

32. – 49. (Canceled).

50. (Currently Amended) A method of fabricating a liquid crystal display (LCD) comprising the steps of:

providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form, each of said thin film transistors fabricated by the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity on the surface of said amorphous silicon layer;

forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer;

subsequently, removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance, and wherein in a sectional view said channel region in said amorphous silicon layer is convex with respect to said contact layer; and

removing the impurity formed over the amorphous silicon layer in the channel region between the drain and source electrodes while retaining the impurity over the amorphous silicon [[film]] layer surface contacted with drain and source region, so that the drain and source regions become a contact layer.

51. (Original) The method of claim 50 wherein said contact layer contains a concentration of said impurity of at least 0.01 %.

52. (Original) The method of claim 50 wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

53. (Cancelled).

54. (Original) The method of claim 50 wherein said diffusion of said impurity into said contact region is performed by heat annealing.

55. (Cancelled).

56. (Original) The method of claim 50 wherein said impurity is phosphorus.

57. (Currently Amended) The method of claim 50 wherein said amorphous silicon [[film]] layer is deposited to a thickness of about 150 nm — 200 nm.

58. – 61. (Canceled).

62. (Currently Amended) A method of fabricating a liquid crystal display (LCD) comprising the steps of:

providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form, each of said thin film transistors fabricated by the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity on the surface of said amorphous silicon layer, wherein said impurity does not diffuse into said amorphous silicon layer;

etching said amorphous silicon layer utilizing a common photoresist to form a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer;

subsequently, removing said impurity from said channel region and then diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance, and wherein in a sectional view said channel region in said amorphous silicon layer is convex with respect to said contact layer; and

removing the impurity formed over the amorphous silicon layer in the channel region between the drain and source electrodes while retaining the impurity over the amorphous silicon [[film]] layer surface contacted with drain and source region, so that the drain and source regions become a contact layer.

63. (Original) The method of claim 62 wherein said contact layer contains a concentration of said impurity of at least 0.01 %.

64. (Original) The method of claim 62 wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

65. (Cancelled).

66. (Original) The method of claim 62 wherein said diffusion of said impurity into said contact region is performed by heat annealing.

67. (Cancelled).

68. (Original) The method of claim 62 wherein said impurity is phosphorus.

69. (Currently Amended) The method of claim 62 wherein said amorphous silicon [[film]] layer is deposited to a thickness of about 150 nm - 200 nm.

70. – 72. (Cancelled).

73. (Currently Amended) A method of fabricating a liquid crystal display (LCD) comprising the steps of:

providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form, each of said thin film transistors fabricated by the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity over said amorphous silicon layer, wherein said amorphous silicon layer does not contain said impurity;

providing a photoresist over said impurity and back exposing said photoresist utilizing said gate stack as a mask and developing a pattern substantially identical with that of said gate;

removing said pattern and forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer;

subsequently, removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance, and wherein in a sectional view said channel region in said amorphous silicon layer is convex with respect to said contact layer; and

removing the impurity formed over the amorphous silicon layer in the channel region between the drain and source electrodes while retaining the impurity over the amorphous silicon [[film]] layer surface contacted with drain and source region, so that the drain and source regions become a contact layer.

74. (Original) The method of claim 73 wherein said contact layer contains a concentration of said impurity of at least 0.01 %.

75. (Original) The method of claim 73 wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

76. (Cancelled).

77. (Original) The method of claim 73 wherein said diffusion of said impurity into said contact region is performed by heat annealing.

78. (Cancelled).

79. (Original) The method of claim 73 wherein said impurity is phosphorus.

80. (Currently Amended) The method of claim 73 wherein said amorphous silicon [[film]] layer is deposited to a thickness of about 150 nm - 200 nm.

81. – 98. (Cancelled).